REMARKS

Claims 1-4 are pending. The Examiner rejects claims 1-4 under 35 U.S.C. § 103(a) over U. S. Patent 5,274,568 to Blinne et al. and U. S. Patent 5,528,511 to Hasegawa. Hasegawa is a newly cited reference and has the same inventor as the present application.

I. Rejection of Claims 1-4 under 35 U.S.C. § 103(a)

Applicant respectfully traverses this rejection.

Applicant's invention as claimed in claims 1-4 is a novel and unobvious system for performing a delay analysis of a logic circuit. One of the features of Applicant's invention as claimed in claims 1-4 is "a delay analysis library" which contains "logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal..."

As with the rejection in the first action based on Blinne in view of Lembach and Jun, Applicant respectfully submits that, again, the Examiner has misinterpreted this claim language. In the previous Action, the Examiner cited Lembach to supply the "logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal..." In the present Action, the Examiner again tries to supply this same deficiency in Blinne, but this time cites Hasegawa. But Hasegawa is not any more relevant to the claim than Lembach or Jun and fails to render the claims obvious.

In particular, the Examiner again acknowledges that Blinne does not teach or suggest storing this "logical operation information" as claimed. Hasegawa does not cure at least these

deficiencies of Blinne. The Examiner asserts that Hasegawa discloses storing this logical operation information in the library. Applicant respectfully disagrees. Hasegawa does not store any logical operation information, and in particular does not store the "logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal..." as required by claims 1-4.

The information stored in Hasegawa is a model information file. The model information file contains a model of the circuit based on graph theory, in which model the circuit is represented by a series of nodes connected by arcs. Each arc has a single start node and end node, with no other nodes in between (column 1, lines 47-57 and Figure 4). Hasegawa also stores in this model information file the delay time for all combinations of the rise and fall of the signal at the start and end nodes for each arc (column 2, lines 6-10 and Figure 6).

As shown in Figures 6 and 8 of Hasegawa, this file does not contain any information showing the correspondence between the input terminals and the output terminal of the logic circuit. The file stores only the delay time information for all combinations of the rise and fall of the signal at the start and end nodes for each arc. For example, Figure 8 shows a delay time of 1 ns for arc b when the signal rises at the start and the end nodes of the arc. The model information file contains no information about the correspondence between the logical values of the input terminals and the output terminal as required by claims 1-4. For at least these reasons, Hasegawa does not cure the deficiencies of Blinne that are acknowledged by the examiner.

Furthermore, it would not have been obvious at the time the invention was made to combine the system of Blinne with Hasegawa to obtain the Applicant's claimed invention because the two references teach incompatible methods for calculating the delay time.

More specifically, Blinne emulates the delay time for a circuit by using a circuit component approach. Blinne combines an edge delay base factor and a edge delay correction factor for each component in the circuit (Blinne, column 3, line 25-30), and then adds the delay times for the individual elements to reach a delay time for the whole circuit. These edge delay factors are computed based on the load capacitance and sensitivity factors present in the elements of the circuit. (Blinne, column 4, line 8-15; Blinne, column 5, line 17-30). Hasegawa computes the delay time by modeling the circuit according to graph theory and determining the delay time for each of the arcs in the graph regardless of whether the arc represents an actual circuit component or not. The two references teach away from each other. The delay analysis methods in Blinne and Hasegawa are incompatible with each other, because the approaches to modeling the circuit are fundamentally different. Because the two references teach away from each other, there clearly would be no motivation to combine the two.

II. Request for Withdrawal of Premature Finality.

Applicant respectfully requests the Examiner to withdraw the premature finality of the rejection. Hasegawa is newly cited art in this action, and notwithstanding the Examiner's assertion to the contrary, Applicant's amendments to the claims did not necessitate the citation of a new reference. These amendments were made to clarify the claim language with respect to 35 U.S.C. § 112, first paragraph. Furthermore, the Examiner's rejection of the claims is based on

an incorrect reading of Hasegawa that is used to supply the same deficiencies in Blinne that were acknowledged in the first action. In the first action, the Examiner incorrectly tried to cure at these deficiencies with Lembach. Therefore, the amendments to the claims cannot be said to have necessitated the citation of a new reference.

For at least these reasons, Applicant respectfully traverses the Examiner's rejection of claims 1-4, and reconsideration and allowance of this application are now believed to be in order. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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